Designation: F 419 – 94

Standard Test Method for Determining Carrier Density in Silicon Epitaxial Layers by Capacitance-Voltage Measurements on Fabricated Junction or Schottky Diodes [1]

This standard is issued under the fixed designation F 419; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ϵ) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This test method covers the measurement of carrier density in silicon epitaxial layers. The precision that can be expected depends upon the carrier-density inhomogeneities parallel and perpendicular to the junction and upon the carrier-density level.

1.2 The measurement requires the formation of Schottky or *p-n* junction diodes on or in the epitaxial layer. In this sense the method is destructive (see, however, 5.2).

1.3 Both *n*- and *p*-type epitaxial layers can be evaluated, on substrates of the same or opposite types, if the layer thickness is greater than twice the zero-bias depletion width plus, for diffused diodes only, the junction depth **(1)**. [2] This test method is also applicable to bulk material.

1.4 This test method covers the carrier density range from about 4×10^{13} to about 8×10^{16} carriers/cm^3(resistivity range from about 0.1 to about 100 Ω·cm in *n*-type wafers and from about 0.24 to about 330 Ω·cm in *p*-type wafers).

1.5 This test method includes procedures for checking both capacitance- and voltage-measuring equipment.

1.6 This test method provides two means of calculating the carrier density from capacitance-voltage data: an incremental method (12.3.1) and a curve-fitting method (12.3.2).

NOTE 1—An alternative method for determining carrier density in epitaxial layers is given in Test Method F 1392. This and a related method, DIN 50 439, use a mercury-probe Schottky barrier contact rather than a fabricated *p-n* junction or Schottky diode. Therefore, measurements by Test Method F 1392 and DIN 50 439 may not be entirely comparable to those made by this test method. DIN 50 439 is also applicable to gallium arsenide as well as to silicon.

1.7 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.* Specific hazard statements are given in 11.8 and 11.14.

2. Referenced Documents

2.1 *ASTM Standards:*

F 95 Test Method for Thickness of Lightly-Doped Silicon Epitaxial Layers on Heavily-Doped Silicon Substrates Using an Infrared Dispersive Spectrophotometer [3]

F 110 Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique [3]

F 723 Practice for Conversion Between Resistivity and Dopant Density for Boron-Doped and Phosphorus-Doped Silicon [3]

F 1392 Test Method for Determining Net Carrier Density Profiles in Silicon Wafers by Capacitance-Voltage Measurements With a Mercury Probe [3]

2.2 *DIN Standard:*

DIN 50 439 Determination of the Dopant Concentration Profile of a Single Crystal Semiconductor Material by Means of the Capacitance-Voltage Method and Mercury Contact [3]

3. Terminology

3.1 *Definitions of Terms Specific to This Standard:*

3.1.1 *breakdown voltage— for the purposes of this test method*, the reverse bias voltage at which the test diode exhibits a leakage current density of 3 mA/cm^2.

4. Summary of Test Method

4.1 The small-signal, high-frequency capacitance of *p-n* junction or Schottky diode is measured as a function of reverse bias voltage. The carrier density as a function of depth is determined from the measured values of capacitance and reverse bias voltage.

5. Significance and Use

5.1 The carrier density is an important material acceptance requirement. In material that is neither too heavily doped nor significantly compensated by impurities of the opposite conductivity type, the resistivity of the epitaxial layer may be determined from the carrier density in accordance with Practice F 723.

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[1] This test method is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

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[2] The boldface numbers in parentheses refer to the list of references at the end of this test method.

[3] *Annual Book of ASTM Standards*, Vol 10.05.

5.2 This test method is suitable for specification acceptance, process control, and research purposes. Because this test method is destructive, measurements are generally made on a sampling basis unless the test diode to be fabricated is made an integral part of the device into which the wafer is being fabricated.

6. Interferences

6.1 Stray inductance and capacitance, caused by excessive lengths of connecting cable, or improper zeroing of the capacitance bridge or meter can cause significant errors in the capacitance measurement. In homogeneous material, such errors result in the calculation of monotonically increasing or decreasing values of carrier density with distance away from the junction.

6.2 Alternating-frequency test sigals greater than 0.05 V rms can lead to errors in the measured capacitance.

7. Apparatus

7.1 Facilities for fabricating *p-n* junction or Schottky diodes on the test specimen.

7.2 *Capacitance Bridge or Meter*, having ranges from 1 to 1000 pF full scale, or greater, in multiples of 10 or less. The measurement frequency shall be in the range from 0.09 to 1.1 MHz inclusive. The accuracy shall be 1.0 % of full scale or better for each range, and the reproducibility shall be 0.25 % of full scale or better. The instrument shall be capable of sustaining external d-c bias of ±200 V or greater and shall be capable of compensating for an external probe fixture with stray capacitance up to 5 pF or greater. The internal a-c measuring signal shall be 0.05 V rms or less.

7.3 *Digital Voltmeter or Potentiometer*, having a sensitivity of 1 mV or better, an accuracy of 0.5 % of full scale or better, a reproducibility of 0.25 % of full scale or better, an input impedance of 100 MΩ or greater, and a common-mode rejection of 100 dB or greater at 60 Hz.

7.4 *D-C Power Supply*, continuously variable, capable of supplying 0 to ±200 V (open circuit) with a ripple of 1 % of the d-c output or less.

7.5 *Curve Tracer*, capable of monitoring the reverse and forward current-voltage characteristics of the diode. The curve tracer shall be capable of applying 200 V at 0.1 mA in the reverse direction and 1.1 V at 1 mA in the forward direction, and have a sensitivity of 10 µA/division or better.

7.6 *Standard Capacitors* of accuracy 0.25 % or better at the measurement frequency. One capacitor shall be in the range from 1 to 10 pF inclusive and one shall be in the range from 10 to 100 pF inclusive.

7.7 *Precision Voltage Source*, capable of providing output voltages from 0 to 200 V. The accuracy of this source shall be 0.1 % of the output voltage or better.

7.8 *Probe Fixture* that holds the specimens containing the diodes; provides probes for making ohmic contact both to the diffused or barrier region, and to the epitaxial layer; and keeps the diode in the dark during the measurement. Vacuum clamping shall be provided. Contact to the epitaxial layer shall be made either by a front-surface contact or, when the layer and substrate are of the same type, by electrical contact to the substrate by means of the vacuum chuck.

7.9 *Toolmaker's Microscope, Shadowgraph, or Planimeter* capable of measuring the junction diameter to an accuracy of 0.5 % or better or the junction area to an accuracy of 1 % or better.

7.10 *Shielded Cables* for making electrical connections between the probe fixture, power supply, capacitance bridge or meter, and digital voltmeter or potentiometer.

8. Sampling

8.1 Because this test method is destructive (see, however, 5.2), it is not generally practical to measure every wafer in a particular lot. A wafer sampling plan shall therefore be agreed upon between the parties to the test.

8.2 If the specimen preparation (see 9.1) involves the fabrication of an array of diodes on a given wafer, it may not be practical to measure every diode on that wafer. A diode sampling plan shall therefore be agreed upon between the parties to the test.

9. Test Specimen

9.1 Fabricate *p-n* junctions or Schottky diodes on the epitaxial layer using planar or mesa technology (see 11.2).

10. Calibration

10.1 Connect shielded cables of a length suitable for measuring the standard capacitors (see 6.1) to the capacitance bridge or meter. Zero the capacitance bridge or meter with the cables connected to the bridge or meter but not to the standard capacitors.

10.2 Connect the cables to one of the standard capacitors; then measure and record the capacitance in picofarads. Disconnect the capacitor.

10.3 Connect the cables to the other standard capacitor; measure and record the capacitance in picofarads. Disconnect the capacitor.

10.4 To verify that the digital voltmeter or potentiometer is within specification over the range from 1 to 200 V, inclusive, use it to measure the precision voltage source at five or more voltages in that range.

10.5 If either the capacitance- or voltage-measuring equipment is not within the required specifications (see 7.2 and 7.3 for values), make necessary adjustments in accordance with the appropriate instrument instruction manuals to bring equipment to within specifications before proceeding with the measurement of the specimen.

11. Procedure

11.1 Unless the epitaxial layer thickness is already known, measure the epitaxial layer thickness by Test Method F 95 or Test Method F 110, depending on whether the layer and substrate are the same or opposite conductivity type, respectively. Estimate the carrier density in the layer to be measured. Consult Ref **(1)** to determine the depletion region width at zero bias. Double this width to allow for the depletion region widening that will occur when the required reverse biases are applied (see 11.13 and 11.14). If a diffused junction diode is to be fabricated, add the anticipated junction depth to this wider depletion width. Make measurements in accordance with the following procedure only if this wider depletion region width