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Standard Guide for Transient Radiation Upset Threshold Testing of Digital Integrated Circuits (Metric)[1]

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1. Scope

1.1 This guide is to assist experimenters in measuring the transient radiation upset threshold of silicon digital integrated circuits exposed to pulses of ionizing radiation greater than 10^3 Gy (matl.)/s.

1.1.1 *Discussion*—This document is intended to be a guide to determine upset threshold, and is not intended to be a stand-alone document.

1.2 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*[2]

E666 Practice for Calculating Absorbed Dose From Gamma or X Radiation

E668 Practice for Application of Thermoluminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices

F1893 Guide for Measurement of Ionizing Dose-Rate Survivability and Burnout of Semiconductor Devices

2.2 *Military Standards:* [3]

Method 1019 in MIL-STD-883. Steady-State Total Dose Irradiation Procedure

Method 1021 in MIL-STD-883. Dose Rate Threshold for Upset of Digital Microcircuits.

3. Terminology

3.1 *Definitions:*

3.1.1 *combinational logic*—A digital logic system with the property that its output state at a given time is solely determined by the logic signals at its inputs at the same time (except for small time delays caused by the propagation delay of internal logic elements).

3.1.1.1 *Discussion*—Combinational circuits contain no internal storage elements. Hence, the output signals are not a function of any signals that occurred at past times. Examples of combinational circuits include gates, adders, multiplexers and decoders.

3.1.2 *latchup condition*—A persistent anomalous high current state in which a parasitic region (for example, a four layer p-n-p-n or n-p-n-p path) is turned on by transient ionizing radiation.

3.1.3 *over-stressed device*—A device that has conducted more than the manufacturer's specified maximum current, or dissipated more than the manufacturer's specified maximum power.

3.1.3.1 *Discussion*—In this case the DUT is considered to be overstressed even if it still meets all of the manufacturer's specifications. Because of the overstress, the device should be evaluated before using it in any high reliability application.

3.1.4 *primary photocurrent (Ipp)*—a transient current flowing from the DUT due to radiation exposure.

3.1.4.1 *Discussion*—The passage of radiation through the depletion region of a semiconductor device creates electron-hole pairs. These electron-hole pairs are then subsequently swept out of the device via the built in potential. This results in a transient current flowing from the DUT due to radiation exposure.

3.1.5 *sequential logic*—A digital logic system with the property that its output state at a given time depends on the sequence and time relationship of logic signals that were previously applied to its inputs.

3.1.5.1 *Discussion*—Examples of sequential logic circuits include flip-flops, shift registers, counters, and arithmetic logic units.

3.1.6 *state vector*—A vector which completely specifies the logic condition of all elements within a logic circuit.

3.1.6.1 *Discussion*—For combinational circuits, the state vector includes the logic signals that are applied to all inputs:

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[2] For referenced ASTM standards, visit the ASTM website, www.astm.org, or contact ASTM Customer Service at service@astm.org. For *Annual Book of ASTM Standards* volume information, refer to the standard's Document Summary page on the ASTM website.

[3] Available from Standardization Documents Order Desk, Bldg. 4, Section D, 700 Robbins Ave., Philadelphia, PA 19111-5094, Attn: NPODS.

for sequential circuits, the state vector must also include the sequence and time relationship of all input signals. In this guide the output states will also be considered part of the state vector definition. For example, an elementary 4-input NAND gate has 16 possible state vectors, 15 of which result in the same output condition ("1" state). A 4-bit counter has 16 possible output conditions, but many more state vectors because of its dependence on the dynamic relationship of various input signals.

3.1.7 *upset response*—The electrical response of a circuit when it is exposed to a pulse of transient ionizing radiation.

3.1.7.1 *Discussion*—Three types of upset response can occur:

(1) transient output error, for which the instantaneous output voltage of an operating digital circuit is greater than a predetermined value (for a low output condition) or less than a predetermined value (for a high output condition), and the circuit spontaneously recovers to its pre-irradiation condition after the radiation pulse subsides. The predetermined values mentioned above are agreed to by all parties participating in the test and should be included in the test plan.

(2) stored logic state error, for which there is a change in the state of one or more internal logic elements that does not recover spontaneously after the radiation pulse. Because the radiation changes the state vector, the circuit spontaneously recovers to a different logic state. This does not imply the change will always be immediately observable on a circuit output. However, the circuit can be restored to its original state vector by re-initializing it afterwards.

(3) functional interrupt error, a circuit wide state in which the circuit ceases functioning as intended. A soft reset may restore functionality to the device. If power cycling is required to restore functionality, the circuit may be in a latched-up state.

3.1.7.2 *Discussion*—Although the term upset response is usually used to describe output voltage responses, some devices, such as open collector gates, are better characterized by measuring the output current. Upset response also includes the transient currents that are induced in the power supply leads (sometimes very large) as well as the response of the device inputs, although in most applications the input response is not significant.

4. Summary of Guide

4.1 For transient radiation upset threshold tests, the transient output voltage and the condition of internal storage elements, or both, is measured at a succession of radiation levels to determine the radiation level for which transient voltage or functional test errors first occur. An oscilloscope, digital storage oscilloscope, transient digitizer or similar instrument is used to measure the output transient voltage. Functional tests are made immediately after irradiation to detect internal changes in state induced by the radiation. The device is initially biased and set up in a predetermined condition. The test conditions are determined from topological analyses or by testing the device in all possible logic state combinations.

4.2 A number of factors are not defined in this guide and must be agreed upon beforehand by the parties to the test. These factors are described in the test plan. As a minimum the test plan must specify the following:

(*1*) Pulse width, energy spectrum, and type of radiation source,

(*2*) Voltage and electrical loading conditions on each pin of the device during testing,

(*3*) Resolution and accuracy required for the upset response threshold of individual devices, along with the method used to vary the radiation level,

(*4*) Failure criterion for transient voltage upset, output current, and power supply current as applicable,

(*5*) Measuring and reporting I_{pp}, transient output voltage and transient output current levels,

(*6*) Functional test to be made after irradiation,

(*7*) Power supply and operating frequency requirements,

(*8*) State vectors used for testing,

(*9*) Radiation levels to use for transient response measurements,

(*10*) Recommended radiation level at which to begin the test sequence, and

(*11*) Procedure to adjust the dose rate during testing.

(*12*) Device temperature during test.

4.3 The state vectors in which the device is to be irradiated are determined from the basic (see 8.2.2) and topological analysis, (see 8.2.3) or both.

5. Significance and Use

5.1 Digital logic circuits are used in system applications where they are exposed to pulses of radiation. It is important to know the minimum radiation level at which transient failures can be induced, since this affects system operation.

6. Interferences

6.1 *Accumulated Ionizing Dose*—Many devices may be permanently damaged by the accumulated ionizing dose they are exposed to during upset testing. This limits the number of radiation pulses that can be applied during transient upset testing. Accumulated ionizing dose sensitivity depends on fabrication techniques and device technology. The maximum ionizing dose to which devices are exposed must not exceed 10 % (see 8.4.5) of the typical ionizing dose failure level of the specific part type.

6.2 *Dosimetry Accuracy*—Since this guide ultimately determines the dose rate at which upset occurs, dosimetry accuracy inherently limits the accuracy of the test result.

6.3 *Latchup*—Some types of integrated circuits may be driven into a latchup condition by transient radiation. If latchup occurs, the device will not function properly until power is temporarily removed and reapplied. Permanent damage may also occur. Although latchup is an important transient response mechanism, this procedure is not applicable to latchup testing. Functional testing after irradiation but without interrupting power is required to detect internal changes of state, and this will also detect latchup.